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UTILITY PATENT APPLICATION TRANSMITTAL
(Large Entity)

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Docket No.
IIZ.008D

Total Pages in this Submission
3

JC625 U.S. PTO 09/398189 09/17/99

TO THE ASSISTANT COMMISSIONER FOR PATENTS
Box Patent Application
Washington, D.C. 20231

Transmitted herewith for filing under 35 U.S.C. 111(a) and 37 C.F.R. 1.53(b) is a new utility patent application for an invention entitled:

SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME

and invented by:

KANAMORI, Jun

If a CONTINUATION APPLICATION, *check appropriate box and supply the requisite information:*

☐ **Continuation** ☒ **Divisional** ☐ **Continuation-in-part (CIP)** of prior application No.: **09/342,751**

Which is a:

☐ **Continuation** ☐ **Divisional** ☐ **Continuation-in-part (CIP)** of prior application No.: _____

Which is a:

☐ **Continuation** ☐ **Divisional** ☐ **Continuation-in-part (CIP)** of prior application No.: _____

Enclosed are:

Application Elements

1. ☒ Filing fee as calculated and transmitted as described below
2. ☒ Specification having **29** pages and including the following:
   - a. ☒ Descriptive Title of the Invention
   - b. ☐ Cross References to Related Applications *(if applicable)*
   - c. ☐ Statement Regarding Federally-sponsored Research/Development *(if applicable)*
   - d. ☐ Reference to Microfiche Appendix *(if applicable)*
   - e. ☒ Background of the Invention
   - f. ☒ Brief Summary of the Invention
   - g. ☒ Brief Description of the Drawings *(if drawings filed)*
   - h. ☒ Detailed Description
   - i. ☒ Claim(s) as Classified Below
   - j. ☒ Abstract of the Disclosure

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Application Elements (Continued)

3. ☒ Drawing(s) *(when necessary as prescribed by 35 USC 113)*

   a. ☒ Formal Number of Sheets 10

   b. ☐ Informal Number of Sheets _____

4. ☒ Oath or Declaration

   a. ☐ Newly executed *(original or copy)* ☐ Unexecuted

   b. ☒ Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional application only)*

   c. ☐ With Power of Attorney ☐ Without Power of Attorney

   d. ☐ *DELETION OF INVENTOR(S)*
   Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. 1.63(d)(2) and 1.33(b).

5. ☒ Incorporation By Reference *(usable if Box 4b is checked)*
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. ☐ Computer Program in Microfiche *(Appendix)*

7. ☐ Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all must be included)*

   a. ☐ Paper Copy

   b. ☐ Computer Readable Copy *(identical to computer copy)*

   c. ☐ Statement Verifying Identical Paper and Computer Readable Copy

Accompanying Application Parts

8. ☐ Assignment Papers *(cover sheet & document(s))*

9. ☐ 37 CFR 3.73(B) Statement *(when there is an assignee)*

10. ☐ English Translation Document *(if applicable)*

11. ☒ Information Disclosure Statement/PTO-1449 ☐ Copies of IDS Citations

12. ☒ Preliminary Amendment

13. ☒ Acknowledgment postcard

14. ☐ Certificate of Mailing

    ☐ First Class ☐ Express Mail *(Specify Label No.):* _____

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Accompanying Application Parts (Continued)

15. ☐ Certified Copy of Priority Document(s) *(if foreign priority is claimed)*

16. ☐ Additional Enclosures *(please identify below):*

Fee Calculation and Transmittal

CLAIMS AS FILED

For	#Filed	#Allowed	#Extra		Rate	Fee
Total Claims	9	- 20 =	0	x	$18.00	$0.00
Indep. Claims	2	- 3 =	0	x	$78.00	$0.00
Multiple Dependent Claims (check if applicable) ☐						$0.00
					BASIC FEE	$760.00
OTHER FEE *(specify purpose)* _____						$0.00
					TOTAL FILING FEE	$760.00

☒ A check in the amount of **$760.00** to cover the filing fee is enclosed.

☒ The Commissioner is hereby authorized to charge and credit Deposit Account No. **50-0238** as described below. A duplicate copy of this sheet is enclosed.

- ☐ Charge the amount of _____ as filing fee.
- ☒ Credit any overpayment.
- ☒ Charge any additional filing fees required under 37 C.F.R. 1.16 and 1.17.
- ☐ Charge the issue fee set in 37 C.F.R. 1.18 at the mailing of the Notice of Allowance, pursuant to 37 C.F.R. 1.311(b).

Signature

Dated: **SEPTEMBER 17, 1999**

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cc:

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	:	
Jun Kanamori	:	Attn: Applications Branch
Serial No. [NEW]	:	Attorney Docket No. IIZ.008D
Filed: September 17, 1999	:	

For: SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME

PRELIMINARY AMENDMENT

Honorable Assistant Commission of Patents and Trademarks,
Washington, D.C. 20231

Sir:

Preliminary to the examination of the above-identified application, please enter the following amendments and remarks.

IN THE SPECIFICATION

Kindly amend the specification as follows:

Page 1, between lines 2 and 3, insert

--CROSS REFERENCE TO RELATED APPLICATIONS

This is a divisional application of application Serial No. 09/342,751, filed June 29, 1999, which is hereby incorporated by reference in its entirety for all purposes.--

IN THE CLAIMS

Please cancel claims 10-18 without prejudice.

REMARKS

By this Preliminary Amendment, the specification has been revised to identify the parent application, and claims 10-18 have been canceled. Entry of this Preliminary Amendment is respectfully requested.

Respectfully submitted,

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Date: September 17, 1999

SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME

TECHNICAL FIELD OF THE INVENTION

The present invention relates to semiconductor fabrication technology, and more particularly to a semiconductor device that is fabricated using SALICIDE (Self Aligned Silicide) process.

BACKGROUND OF THE INVENTION

In recent years, semiconductor devices have been miniaturized and improved in performance, and at the same time, system LSIs have been proposed. In such a system LSI, for improving its performance, it is required to decrease resistance of a gate pattern and active regions of source and drain. As shown in "Semiconductor World", May 1998, page 66, salicide process has been used to decrease that resistance. Especially for SOI (Silicon-On-Insulator) type of devices, the salicide process is important. SOI technology has become increasingly important in the field of integrated circuits. In SOI fabrication, a layer of semiconductor material overlies an insulating layer, typically, a single crystal layer of silicon overlies a layer of silicon dioxide, which itself overlies a silicon substrate.

According to a conventional method, a BOX (Buried Oxide) layer is formed on a silicon substrate. Next, a filed oxide layer and a

SOI (Silicon on Insulator) layer are formed on the BOX layer. The SOI layer is usually designed to have a thickness of 50nm to 100nm. A gate oxide layer is formed on the SOI layer, and a poly-silicon gate layer is formed on the gate oxide layer. A gate side wall layer is formed on the SOI layer to surround the poly-silicon gate layer and gate oxide layer.

Before a first RTA (Rapid Thermal Annealing) process, thus fabricated structure is covered with Co (cobalt) layer and TiN (Titanium Nitride) layer. In the first RTA process, silicide reaction occurs at the junction area between the SOI layer and the Co layer, and between the poly-silicon gate layer and the Co layer, so that the SOI layer and gate layer are silicided. The silicide regions are of CoSi, which still have a high resistance. After the first RTA process, the remaining metal (Co and TiN) are selectively removed by a wet process using such as ammonia water or hydrogen peroxide solution.

Next, the second RTA process is carried out so that silicon in the SOI layer and poly-silicon gate layer again react with the silicide regions. As a result, the silicide regions become to be of $CoSi_2$, which have lower resistance.

According to the above described conventional method, low resistance wiring can be realized by the salicide process. For more improving performance of SOI devices, it is required to make the SOI layer much thinner, for example less than 70nm. If the SOI layer is formed to have irregular thickness, thinner part of the SOI layer may

be salicided entirely and voids may be made in the SOI layer. If voids are made in the SOI layer, the BOX layer may be etched when contact holes are formed on the active areas. If the silicon substrate is etched as well in worst case, the silicon substrate is electrically connected to the upper electrode. As a result, undesirable electrical leakage is made.

OBJECTS OF THE INVENTION

Accordingly, an object of the present invention is to improve quality of a semiconductor device even if a SOI layer is designed to be very thin.

Additional objects, advantages and novel features of the present invention will be set forth in part in the description that follows, and in part will become apparent to those skilled in the art upon examination of the following or may be learned by practice of the invention. The objects and advantages of the invention may be realized and attained by means of the instrumentalities and combinations particularly pointed out in the appended claims.

SUMMARY OF THE INVENTION

According to a first aspect of the present invention, in a method for fabricating a semiconductor device, a silicide material is formed at least on the surface of an area to be silicided. Then, a first RTA (Rapid Thermal Annealing) process is performed to form a first-

reacted silicide region. Next, a supplemental silicon layer is formed over the entire surface; and a second RTA process is performed to form a second-reacted silicide region.

The main feature of the present invention is to form the supplemental silicon layer over the entire surface prior to the second RTA process. According to the present invention, silicon for silicide process is also provided from the supplemental silicon layer in the second RTA process. As a result, low resistance wiring can be well realized by the salicide process even if an SOI layer is formed to be thinner. Consequently, the fabricated semiconductor device is prevented from having a problem of electrical leakage.

The silicide material may include cobalt (Co) or titanium (Ti). The supplemental silicon layer may be of poly-silicon formed by CVD (Chemical Vapor Deposition) technique. The supplemental silicon layer may be of a-Si (amorphousness silicon) formed by sputtering technique.

An impurity may be doped into the supplemental silicon layer before the second RTA process, wherein the impurity is of the same type as active regions. When such an impurity is doped into the supplemental silicon layer, the remaining (non-reacted) silicon can be removed at a high etching rate and high selectivity after the second RTA process. Further, the type of impurity is the same as that of the impurity doped into the corresponding active region, so that the silicide reaction progresses smoothly.

The impurity may be doped into one of N-channel region and P-channel region. When impurity is doped one of N and P channel regions, the silicide reaction can be well controlled between the N-channel region and P-channel region.

According to a second aspect of the present invention, a semiconductor device is fabricated by the above described method of the first aspect of the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1A to 1C are cross-sectional views showing fabrication steps of a semiconductor device according to a conventional technique.

Figs. 2A to 2E are cross-sectional views showing fabrication steps of a semiconductor device according to a first preferred embodiment of the present invention.

Figs. 3A to 3E are cross-sectional views showing fabrication steps of a semiconductor device according to a second preferred embodiment of the present invention.

Figs. 4A to 4E are cross-sectional views showing fabrication steps of a semiconductor device according to a third preferred embodiment of the present invention.

Figs. 5A to 5D are cross-sectional views showing fabrication steps of a semiconductor device according to a fourth preferred embodiment of the present invention.

Figs. 6A to 6C are cross-sectional views showing fabrication

steps of a semiconductor device according to a fifth preferred embodiment of the present invention.

DETAILED DISCLOSURE OF THE INVENTION

For better understanding of the present invention, a conventional technology is first described. Figs. 1A to 1C are cross-sectional views showing fabrication steps of a conventional semiconductor device. Figs. 1A to 1C show salicide process of a SOI (Silicon on Insulator) type of semiconductor device.

Fig. 1A shows a condition in which gate-side-wall process is completed. As shown in Fig. 1A, a BOX (Buried Oxide) layer 14 is formed on a silicon substrate 12 to have a thickness of 100nm to 200nm. A filed oxide layer 16 and a SOI (Silicon on Insulator) layer 18 are formed on the BOX layer 14. The SOI layer 18 is of FD (Fully Depletion) type and is designed to have a thickness of 50nm to 100nm. A gate oxide layer 20 is formed on the SOI layer 18 to have a thickness of 3.5nm to 7.0nm. A poly-silicon gate layer 22 is formed on the gate oxide layer 20 to have a thickness of 150nm to 250nm. A gate side wall layer 24 is formed on the SOI layer 18 to surround the poly-silicon gate layer 22 and gate oxide layer 20. The gate side wall layer 24 is designed to have a width of 80nm to 150nm.

Fig. 1B shows a condition in that the structure, shown in Fig. 1A, is covered with Co (cobalt) layer 26 and TiN (Titanium Nitride) layer 28 by sputtering process. The Co layer 26 is formed over the

entire structure to have a thickness of 5nm to 12nm. The TiN layer 28 is formed over the Co layer 26 to have a thickness of 5nm to 10nm. The TiN layer 28 functions for controlling salicide process.

Fig. 1C shows a condition in that first and second RTA (Rapid Thermal Annealing) processes are carried out to the structure, shown in Fig. 1B. In the first RTA process of 500 to 600℃, silicide reaction occurs at the junction area between the SOI layer 18 and the Co layer 26, and between the poly-silicon gate layer 22 and the Co layer 26, so that silicide regions 30 and 32 are formed.

After the first RTA process, the remaining metal (Co and TiN) are selectively removed by a wet process using such as ammonia water or hydrogen peroxide solution. The silicide regions 30 and 32 are of CoSi, which still have a high resistance.

Next, the second RTA process is carried out at a temperature of 750 to 850℃ so that silicon in the SOI layer 18 and poly-silicon gate layer 22 again react with the silicide regions 30 and 32, respectively. As a result, the silicide regions 30 and 32 become to be of $CoSi_2$, which have lower resistance.

According to the above described conventional method, low resistance wiring can be realized by the salicide process. For more improving performance of SOI devices, it is required to make the SOI layer 18 much thinner, for example less than 70nm. If the SOI layer 18 is formed to have irregular thickness, thinner part of the SOI layer 18 may be salicided entirely and voids may be made in the SOI layer

18. If voids are made in the SOI layer 18, the BOX layer 14 may be etched when contact holes are formed on the active area (30). If the silicon substrate 12 is etched as well in worst case, the silicon substrate 12 is electrically connected to the upper electrode. As a result, undesirable electrical leakage is made.

Figs. 2A to 2E are cross-sectional views showing fabrication steps of a semiconductor device according to a first preferred embodiment of the present invention. Figs. 2A to 2E show salicide process of a SOI (Silicon on Insulator) type of semiconductor device.

Fig. 2A shows a condition in which gate-side-wall process is completed. As shown in Fig. 2A, a BOX (Buried Oxide) layer 114 is formed on a silicon substrate 112 to have a thickness of 100nm to 200nm. A filed oxide layer 116 and a SOI (Silicon on Insulator) layer 118 are formed on the BOX layer 114. The SOI layer 118 is of FD (Fully Depletion) type and is designed to have a thickness of 50nm to 100nm. A gate oxide layer 120 is formed on the SOI layer 118 to have a thickness of 3.5nm to 7.0nm. A poly-silicon gate layer 122 is formed on the gate oxide layer 120 to have a thickness of 150nm to 250nm. A gate side wall layer 124 is formed on the SOI layer 118 to surround the poly-silicon gate layer 122 and gate oxide layer 120. The gate side wall layer 124 is designed to have a width of 80nm to 150nm.

Fig. 2B shows a condition in that the structure, shown in Fig. 2A, is covered with Co (cobalt) layer 126 and TiN (Titanium Nitride)

layer 128 by sputtering process. The Co layer 126 is formed over the entire structure to have a thickness of 5nm to 12nm. The TiN layer 128 is formed over the Co layer 126 to have a thickness of 5nm to 10nm. The TiN layer 128 functions for controlling salicide process.

Fig. 2C shows a condition in that a first RTA (Rapid Thermal Annealing) process is carried out to the structure. The first RTA process is carried out at 500 to 600℃, so that silicide reaction occurs at the junction area between the SOI layer 118 and the Co layer 126, and between the poly-silicon gate layer 122 and the Co layer 126. As a result of the first RTA process, silicide regions 130 and 132 are formed. The silicide regions 130 and 132 can be called "higher-resistance silicide regions" or "first-reacted silicide regions". The silicide regions 130 and 132 are of CoSi, which still have a higher resistance. After the first RTA process, the remaining metal (Co and TiN) are selectively removed by a wet process using such as ammonia water or hydrogen peroxide solution.

Before a second RTA process, a poly-silicon layer 136 is formed over the entire structure, as a supplemental silicon layer, as shown in Fig. 2D. The poly-silicon layer 136 is formed by CVD (Chemical Vapor Deposition) process at a temperature of 350 to 500℃ to have a thickness of 5nm to 10nm.

Next, a second RTA process is carried out at a temperature of 750 to 850℃. In the second RTA process, silicon contained in the SOI layer 118 and poly-silicon layer 136 reacts with the silicide region

130, while silicon contained in the poly-silicon gate layer 122 and the poly-silicon layer 136 reacts with the silicide region 132. According to this embodiment, silicon for silicide process is provided not only from the SOI layer 118 and the poly-silicon gate layer 122 but also from the poly-silicon layer 136. Therefore, enough amount of silicon remains in the SOI layer 118 even after the second RTA process. As a result of the second RTA process, silicide regions 138 and 140 of $CoSi_2$, which have lower resistance, are formed. The silicide regions 138 and 140 can be called "lower-resistance silicide regions" or "second-reacted silicide regions".

After the second RTA process, the remaining metal (Co and TiN) are selectively removed from the silicide regions 138 and 140. Such removing process can be carried out by a wet process (dipping) using aquafortis or by plasma etching using a chlorine system gas or a fluorine system gas.

According to the first preferred embodiment, silicon for silicide process is provided not only from the SOI layer 118 and the poly-silicon gate layer 112 but also from the poly-silicon layer 136. As a result, enough amount of silicon remains in the SOI layer 118 after the second RTA process; and therefore, low resistance wiring can be realized by the salicide process even if the SOI layer 118 is formed to be much thinner, for example less than 70nm. In other words, the BOX layer 114 is prevented from being etched when contact holes are formed on the active area (130). Consequently, the fabricated

semiconductor device is prevented from having a problem of electrical leakage.

Figs. 3A to 3E are cross-sectional views showing fabrication steps of a semiconductor device according to a second preferred embodiment of the present invention. Figs. 2A to 2E show salicide process of a SOI (Silicon on Insulator) type of semiconductor device. According to the second preferred embodiment, an a-Si (amorphousness silicon) layer is formed before second RTA process instead of the poly-silicon layer 136, shown in Fig. 2D, in the first preferred embodiment.

Fig. 3A shows a condition in which gate-side-wall process is completed. As shown in Fig. 3A, a BOX (Buried Oxide) layer 214 is formed on a silicon substrate 212 to have a thickness of 100nm to 200nm. A filed oxide layer 216 and a SOI (Silicon on Insulator) layer 218 are formed on the BOX layer 214. The SOI layer 218 is of FD (Fully Depletion) type and is designed to have a thickness of 50nm to 100nm. A gate oxide layer 220 is formed on the SOI layer 218 to have a thickness of 3.5nm to 7.0nm. A poly-silicon gate layer 222 is formed on the gate oxide layer 220 to have a thickness of 150nm to 250nm. A gate side wall layer 224 is formed on the SOI layer 218 to surround the poly-silicon gate layer 222 and gate oxide layer 220. The gate side wall layer 224 is designed to have a width of 80nm to 150nm.

Fig. 3B shows a condition in that the structure, shown in Fig.

3A, is covered with Co (cobalt) layer 226 and TiN (Titanium Nitride) layer 228 by sputtering process. The Co layer 226 is formed over the structure to have a thickness of 5nm to 12nm. The TiN layer 228 is formed over the Co layer 226 to have a thickness of 5nm to 10nm. The TiN layer 228 functions for controlling salicide process.

Fig. 3C shows a condition in that a first RTA (Rapid Thermal Annealing) process is carried out to the structure. The first RTA process is carried out at 500 to 600℃, so that silicide reaction occurs at the junction area between the SOI layer 218 and the Co layer 226, and between the poly-silicon gate layer 222 and the Co layer 226. As a result of the first RTA process, silicide regions 230 and 232 are formed. The silicide regions 230 and 232 can be called "higher-resistance silicide regions" or "first-reacted silicide regions". The silicide regions 230 and 232 are of CoSi, which still have a higher resistance. After the first RTA process, the remaining metal (Co and TiN) are selectively removed by a wet process using such as ammonia water or hydrogen peroxide solution.

Before a second RTA process, an a-Si layer 236 is formed over the entire structure, as a supplemental silicon layer, as shown in Fig. 3D. The a-Si layer 236 is formed by sputtering process.

Next, a second RTA process is carried out at a temperature of 750 to 850℃. In the second RTA process, silicon contained in the SOI layer 218 and a-Si layer 236 again reacts with the silicide region 130, while silicon contained in the poly-silicon gate layer 222 and the

a-Si layer 236 again reacts with the silicide region 232. According to this embodiment, silicon for silicide process is provided not only from the SOI layer 218 and the poly-silicon gate layer 222 but also from the a-Si layer 236. Therefore, enough amount of silicon remains in the SOI layer 218 even after the second RTA process. As a result of the second RTA process, silicide regions 238 and 240 of $CoSi_2$, which have lower resistance, are formed. The silicide regions 238 and 240 can be called "lower-resistance silicide regions" or "second-reacted silicide regions".

After the second RTA process, the remaining metal (Co, TiN and a-Si) are selectively removed from the silicide regions 238 and 240. Such removing process can be carried out by a wet process (dipping) using aquafortis or by plasma etching using a chlorine system gas or a fluorine system gas.

According to the second preferred embodiment, silicon for silicide process is provided not only from the SOI layer 218 and the poly-silicon gate layer 212 but also from the a-Si layer 236. As a result, enough amount of silicon remains in the SOI layer 218 after the second RTA process; and therefore, low resistance wiring can be realized by the salicide process even if the SOI layer 218 is formed to be much thinner, for example less than 70nm. In other words, the BOX layer 214 is prevented from being etched when contact holes are formed on the active area (230). Consequently, the fabricated semiconductor device is prevented from having a problem of electrical

leakage. Comparing to the first preferred embodiment, the a-Si layer 236 can be formed by a process at a lower temperature (less than 200℃). Thus, a silicide reaction is more efficiently prevented from undesirably progressing before the second RTA process.

Figs. 4A to 4E are cross-sectional views showing fabrication steps of a semiconductor device according to a third preferred embodiment of the present invention. Figs. 4A to 4E show salicide process of a SOI (Silicon on Insulator) type of semiconductor device. According to the third preferred embodiment, a Ti (titanium) layer is formed before a first RTA process instead of the Co layer 126 (226), shown in Fig. 2B and 3B, in the first and second preferred embodiments.

It is known that Titanium and Cobalt reacts with silicon in the different manner. When using titanium for salicide process, a $TiSi_2$ is formed in the first RTA process. Then, in the second RTA process, phase transition of C49 to C54 occurs in the silicide regions, so that the resistance of the silicide regions is lowered.

Fig. 4A shows a condition in which gate-side-wall process is completed. As shown in Fig. 4A, a BOX (Buried Oxide) layer 314 is formed on a silicon substrate 312 to have a thickness of 100nm to 200nm. A filed oxide layer 316 and a SOI (Silicon on Insulator) layer 318 are formed on the BOX layer 314. The SOI layer 318 is of FD (Fully Depletion) type and is designed to have a thickness of 50nm to 100nm. A gate oxide layer 320 is formed on the SOI layer 318 to

have a thickness of 3.5nm to 7.0nm. A poly-silicon gate layer 322 is formed on the gate oxide layer 320 to have a thickness of 150nm to 250nm. A gate side wall layer 324 is formed on the SOI layer 318 to surround the poly-silicon gate layer 322 and gate oxide layer 320. The gate side wall layer 324 is designed to have a width of 80nm to 150nm.

Fig. 4B shows a condition in that the structure, shown in Fig. 4A, is covered with Ti (titanium) layer 326 and TiN (Titanium Nitride) layer 328. The Ti layer 326 is formed over the entire structure, and the TiN layer 328 is formed over the Co layer 326. The TiN layer 328 functions for controlling salicide process.

Fig. 4C shows a condition in that a first RTA (Rapid Thermal Annealing) process is carried out to the structure. The first RTA process is carried out at 500 to 600℃, so that silicide reaction occurs at the junction areas between the SOI layer 318 and the Ti layer 326, and between the poly-silicon gate layer 322 and the Ti layer 326. As a result of the first RTA process, silicide regions 330 and 332 are formed. The silicide regions 330 and 332 can be called "higher-reacted silicide regions" or "first-reacted silicide regions". The silicide regions 330 and 332 are of $TiSi_2$ (C49), which still have a higher resistance. A part of the silicide regions 330 and 332 does not become to be of $TiSi_2$ (C49) but of TiSi. After the first RTA process, the remaining metal (Ti and TiN) are selectively removed by a wet process using such as ammonia water or hydrogen peroxide solution.

Before a second RTA process, a poly-Si (or a-Si) layer 336 is formed over the entire structure, as a supplemental silicon layer, as shown in Fig. 4D. Then, a second RTA process is carried out at a temperature of 800 to 850℃. In the second RTA process, phase transition of $TiSi_2$ (C49) to $TiSi_2$ (C54) occurs in the silicide regions 320 and 332, so that the resistance of the silicide regions 320 and 330 is lowered. In other words, silicide regions 338 and 340 of $TiSi_2$ (C54) are formed. Incomplete silicide regions of TiSi are changed into of $TiSi_2$. The silicide regions 338 and 340 can be called "lower-resistance silicide regions" or "second-reacted silicide regions".

After the second RTA process, the remaining metal (Co, TiN and poly-Si/a-Si) are selectively removed, as shown in Fig. 4E. Such removing process can be carried out by a wet process (dipping) using aquafortis or by plasma etching using a chlorine system gas or a fluorine system gas.

According to the third preferred embodiment, silicon for silicide process is provided not only from the SOI layer 318 and the poly-silicon gate layer 312 but also from the poly-Si/a-Si layer 336. As a result, enough amount of silicon remains in the SOI layer 318 after the second RTA process; and therefore, low resistance wiring can be realized by the salicide process even if the SOI layer 318 is formed to be much thinner. In other words, the BOX layer 314 is prevented from being etched when contact holes are formed on the active area (330). Consequently, the fabricated semiconductor device is

prevented from having a problem of electrical leakage.

Figs. 5A to 5D are cross-sectional views showing fabrication steps of a semiconductor device according to a fourth preferred embodiment of the present invention. Figs. 5A to 5D show salicide process of a SOI (Silicon on Insulator) type of semiconductor device. According to the fourth preferred embodiment, impurities, which are different between N-channel region and P-channel region, are doped into a supplemental silicon layer. In the above described first to third preferred embodiments, the same type of supplemental silicon layers (136, 236 and 336) are used both for N-channel region and P-channel region.

Fig. 5A shows a condition in which a first RTA process is completed and a supplemental silicon layer (436) is formed over the entire structure. As shown in Fig. 5A, a BOX (Buried Oxide) layer 414 is formed on a silicon substrate 412 to have a thickness of 100nm to 200nm. A filed oxide layer 416 and a SOI (Silicon on Insulator) layer 418 are formed on the BOX layer 414. The SOI layer 418 is of FD (Fully Depletion) type and is designed to have a thickness of 50nm to 100nm. A gate oxide layer 420 is formed on the SOI layer 418 to have a thickness of 3.5nm to 7.0nm. A poly-silicon gate layer 422 is formed on the gate oxide layer 420 to have a thickness of 150nm to 250nm. A gate side wall layer 424 is formed on the SOI layer 418 to surround the poly-silicon gate layer 422 and gate oxide layer 420. The gate side wall layer 424 is designed to have a width of 80nm to

150nm.

Although not shown in Fig. 5A, the structure is covered with Co (cobalt) layer and TiN (Titanium Nitride) layer by sputtering process. The Co layer is formed over the structure to have a thickness of 5nm to 12nm. The TiN layer is formed over the Co layer to have a thickness of 5nm to 10nm. The TiN layer functions for controlling salicide process.

Next, a first RTA (Rapid Thermal Annealing) process is carried out at a temperature of 500 to 600℃, so that silicide reaction occurs at the junction area between the SOI layer 418 and the Co layer, and between the poly-silicon gate layer 422 and the Co layer. As a result of the first RTA process, silicide regions 430 and 432 are formed. The silicide regions 430 and 432 can be called "lower-resistance silicide regions" or "first-reacted silicide regions". The silicide regions 430 and 432 are of CoSi, which still have a higher resistance. After the first RTA process, the remaining metal (Co and TiN) are selectively removed by a wet process using such as ammonia water or hydrogen peroxide solution.

Before a second RTA process, a poly-Si layer 436 is formed over the entire structure, as a supplemental silicon layer, as shown in Fig. 5A.

Next, the P-channel region is covered with a photo-resist layer 450, as shown in Fig. 5B. Then, N type impurity, such as P (phosphorus) or As (arsenic), is doped into the poly-Si layer 436 at the

N-channel region by ion-implant technique to make a N-doped silicon layer 436N. In the doping process, the N type impurity is also doped into the photo-resist layer 450. After the doping process, the remaining photo-resist 450 is removed by a predetermined process.

Next, the N-channel region is covered with a photo-resist layer 452, as shown in Fig. 5C. Then, P type impurity, such as B (boron), is doped into the poly-Si layer 436 at the P-channel region by ion-implant technique to make a P-doped silicon layer 436P. In the doping process, the P type impurity is also doped into the photo-resist layer 452. After the doping process, the remaining photo-resist 450 is removed by a predetermined process.

Next, a second RTA process is carried out to the entire structure, as shown in Fig. 5D. With the second RTA process, low resistance silicide regions 438 and 440 are formed, in the same manner as the first to third preferred embodiments. The silicide regions 438 and 440 can be called "lower-resistance silicide regions" or "second-reacted silicide regions". After the second RTA process, the remaining metal (Co, TiN and poly-Si/a-Si) are selectively removed by a wet process (dipping) using aquafortis or by plasma etching using a chlorine system gas or a fluorine system gas.

According to the fourth preferred embodiment of the present invention, impurities are doped into the supplemental silicon layer 436, so that the remaining silicon after the second RTA process can be removed at a high etching rate and high selectivity. Such advantage

is especially good in the case of dry etching process. Further, the type of impurity doped into the supplemental silicon layer 436 is the same as that of the impurity doped into the corresponding active regions (430), so that the silicide reaction progresses smoothly.

Figs. 6A to 6C are cross-sectional views showing fabrication steps of a semiconductor device according to a fifth preferred embodiment of the present invention. Figs. 6A to 6C show salicide process of a SOI (Silicon on Insulator) type of semiconductor device. According to the fifth preferred embodiment, impurity is doped into a supplemental silicon layer (536) only in a N-channel region. In the same manner, impurity can be doped into a supplemental silicon layer (536) only in a P-channel region.

Fig. 6A shows a condition in which a first RTA process is completed and a supplemental silicon layer (536) is formed over the entire structure. As shown in Fig. 6A, a BOX (Buried Oxide) layer 514 is formed on a silicon substrate 512 to have a thickness of 100nm to 200nm. A filed oxide layer 516 and a SOI (Silicon on Insulator) layer 518 are formed on the BOX layer 514. The SOI layer 518 is of FD (Fully Depletion) type and is designed to have a thickness of 50nm to 100nm. A gate oxide layer 520 is formed on the SOI layer 518 to have a thickness of 3.5nm to 7.0nm. A poly-silicon gate layer 522 is formed on the gate oxide layer 520 to have a thickness of 150nm to 250nm. A gate side wall layer 524 is formed on the SOI layer 518 to surround the poly-silicon gate layer 522 and gate oxide layer 520.

The gate side wall layer 524 is designed to have a width of 80nm to 150nm.

Then, in the same manner as the fourth preferred embodiment, a first RTA process is carried out. As a result of the first RTA process, silicide regions 530 and 532 are formed. The silicide regions 530 and 532 can be called "higher-resistance silicide regions" or "first-reacted silicide regions". The silicide regions 530 and 532 are of CoSi, which still have a higher resistance. After the first RTA process, the remaining metal (Co and TiN) are selectively removed by a wet process using such as ammonia water or hydrogen peroxide solution. Then, a poly-Si layer 536 is formed over the entire structure.

Next, the P-channel region is covered with a photo-resist layer 550, as shown in Fig. 6B. Then, N type impurity, such as P (phosphorus) or As (arsenic), is doped into the a-Si layer 536 at the N-channel region by ion-implant technique to make a N-doped silicon layer 536N. In the doping process, the N type impurity is also doped into the photo-resist layer 550. After the doping process, the remaining photo-resist 550 is removed by a predetermined process.

Next, a second RTA process is carried out to the entire structure, as shown in Fig. 6C. With the second RTA process, low resistance silicide regions 538 and 540 are formed, in the same manner as the first to fourth preferred embodiments. The silicide regions 538 and 540 can be called "lower-resistance silicide regions" or

"second-reacted silicide regions". After the second RTA process, the remaining metal (Co, TiN and poly-Si/a-Si) are selectively removed by a wet process (dipping) using aquafortis or by plasma etching using a chlorine system gas or a fluorine system gas.

According to the fifth preferred embodiment of the present invention, impurity is doped into the supplemental silicon layer 536 in one of N and P channel regions, so that the silicide reaction can be well controlled between the N-channel region and P-channel region.

What is claimed is:

1. A method for fabricating a semiconductor device using a salicide (self aligned silicide) process, comprising the steps of:

providing a material to be silicided at least on the surface of an area to be silicided;

performing a first RTA (Rapid Thermal Annealing) process to form a first-reacted silicide region;

providing a supplemental silicon layer over the surface; and

performing a second RTA process to form a second-reacted silicide region.

2. A method according to claim 1, wherein

the material comprises cobalt (Co).

3. A method according to claim 1, wherein

the material comprises titanium (Ti).

4. A method according to claim 1, wherein

the supplemental silicon layer is of poly-silicon formed by CVD (Chemical Vapor Deposition) technique.

5. A method according to claim 1, wherein

the supplemental silicon layer is of a-Si (amorphousness silicon)

formed by sputtering technique.

6. A method according to claim 1, further comprising the step of:

selectively removing non-reacted silicon from the second-reacted silicide region after the second RTA process.

7. A method according to claim 1, further comprising the step of:

doping an impurity into the supplemental silicon layer before the second RTA process, wherein

the impurity is of the same type as active regions.

8. A method according to claim 7, wherein

the impurity is doped into one of N-channel region and P-channel region.

9. A method for fabricating a semiconductor device using a salicide (self aligned silicide) process, comprising the steps of:

providing a silicon substrate;

providing a BOX (Buried Oxide) layer in the silicon substrate;

providing a filed oxide layer and a SOI (Silicon on Insulator) layer on the BOX layer;

providing a gate oxide layer on the SOI layer;

providing a poly-silicon gate layer on the gate oxide layer;

providing a gate side wall layer on the SOI layer to surround the poly-silicon gate layer and gate oxide layer;

providing a material to be silicided on the surface;

performing a first RTA (Rapid Thermal Annealing) process to form first-reacted silicide regions in the poly-silicon gate layer and source/drain active areas of the SOI layer;

removing non-reacted material from the first-reacted silicide regions;

providing a supplemental silicon layer over the entire surface;

performing a second RTA process so that the first-reacted silicide regions react again with the supplemental silicon layer to form second-reacted silicide regions; and

selectively removing non-reacted silicon from the second-reacted silicide regions.

10. A semiconductor device that is fabricated by a method comprising the steps of:

providing a material to be silicided at least on the surface of an area to be silicided;

performing a first RTA (Rapid Thermal Annealing) process to form a first-reacted silicide region;

providing a supplemental silicon layer over the entire surface; and

performing a second RTA process to form a second-reacted silicide region.

11. A semiconductor device according to claim 10, wherein the silicide material comprises cobalt (Co).

12. A semiconductor device according to claim 10, wherein the silicide material comprises titanium (Ti).

13. A semiconductor device according to claim 10, wherein the supplemental silicon layer is of poly-silicon formed by CVD (Chemical Vapor Deposition) technique.

14. A semiconductor device according to claim 10, wherein the supplemental silicon layer is of a-Si (amorphousness silicon) formed by sputtering technique.

15. A semiconductor device according to claim 10, wherein non-reacted silicon is selectively removed from the second-reacted silicide region after the second RTA process.

16. A semiconductor device according to claim 10, wherein

an impurity is doped into the supplemental silicon layer before the second RTA process, and

the impurity is of the same type as active regions.

17. A semiconductor device according to claim 16, wherein

the impurity is doped into one of N-channel region and P-channel region.

18. A semiconductor device that is fabricated by a method comprising the steps of:

providing a silicon substrate;

providing a BOX (Buried Oxide) layer in the silicon substrate;

providing a filed oxide layer and a SOI (Silicon on Insulator) layer on the BOX layer;

providing a gate oxide layer on the SOI layer;

providing a poly-silicon gate layer on the gate oxide layer;

providing a gate side wall layer on the SOI layer to surround the poly-silicon gate layer and gate oxide layer;

providing a material to be silicided on the surface;

performing a first RTA (Rapid Thermal Annealing) process to form first-reacted silicide regions in the poly-silicon gate layer and source/drain active areas of the SOI layer;

removing non-reacted material from the first-reacted silicide

regions;

providing a supplemental silicon layer over the entire surface;

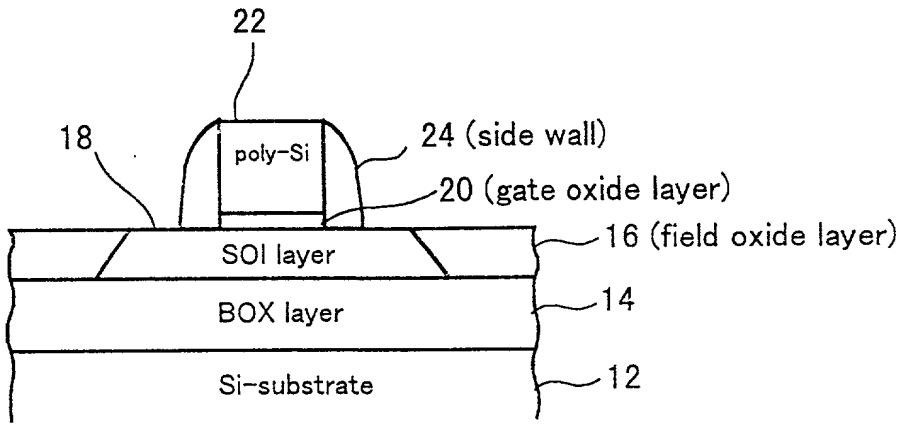
performing a second RTA process so that the first-reacted silicide regions react again with the supplemental silicon layer to form second-reacted silicide regions; and

selectively removing non-reacted silicon from the second-reacted silicide regions.

ABSTRACT OF THE DISCLOSURE

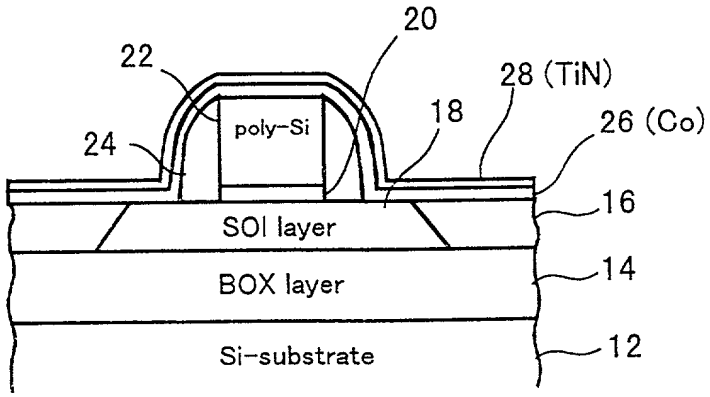
In a method for fabricating a semiconductor device, a silicide material is formed at least on the surface of an area to be silicided. Then, a first RTA (Rapid Thermal Annealing) process is performed to form a first-reacted silicide region. Next, a supplemental silicon layer is formed over the entire surface; and a second RTA process is performed to form a second-reacted silicide region.

FIG. 1A
(PRIOR ART)



Sputtering
(TiN, Co)

FIG. 1B
(PRIOR ART)



1st & 2nd RTA

FIG. 1C
(PRIOR ART)

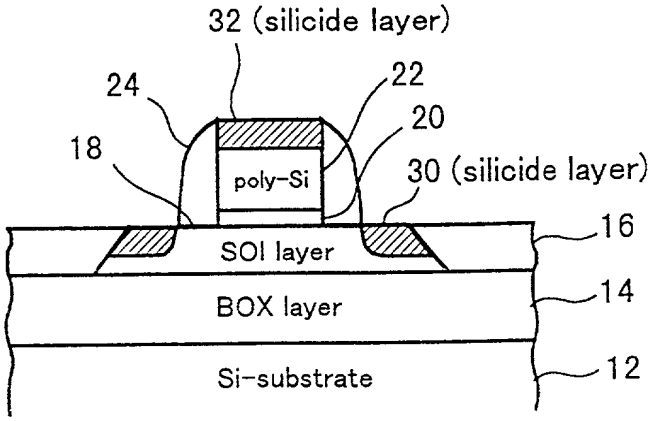


FIG. 2A

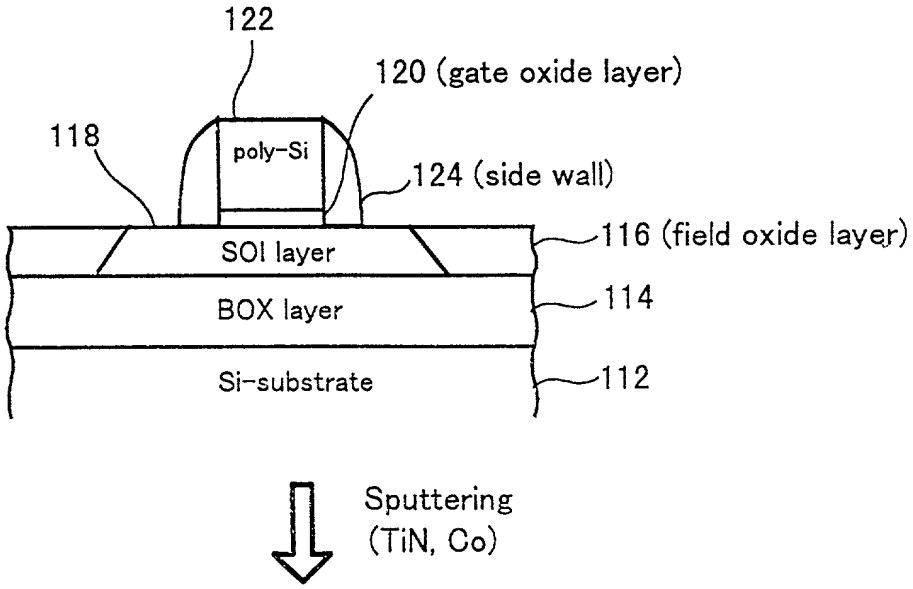


FIG. 2B

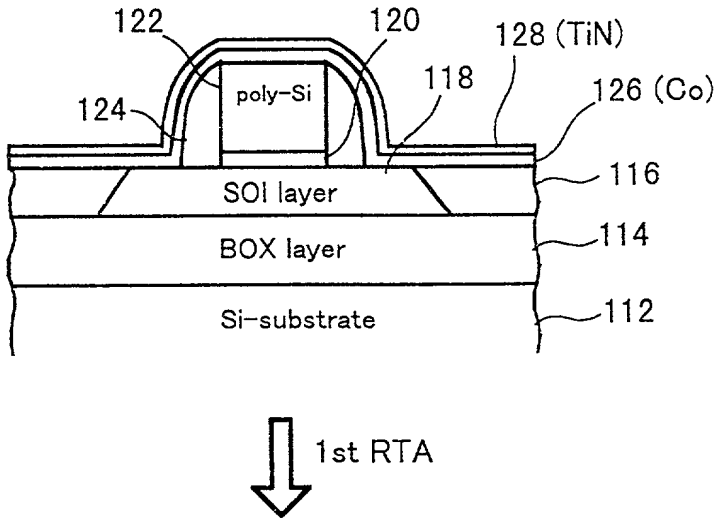


FIG. 2C

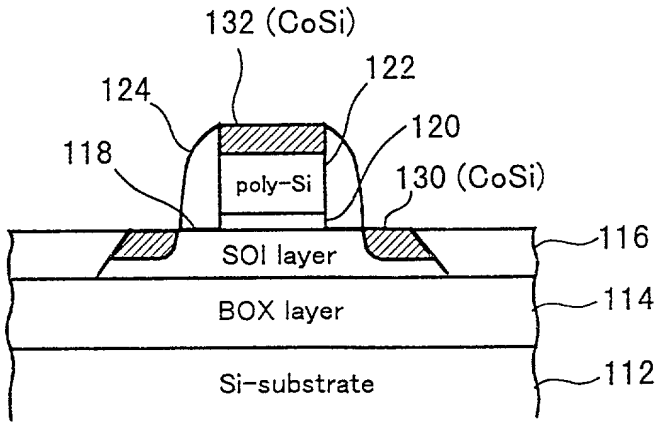


FIG. 2D

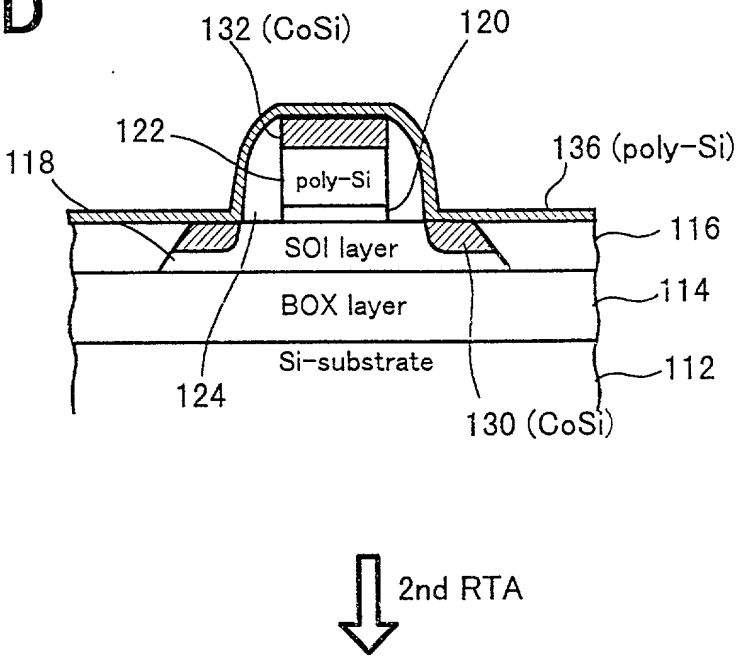

132 (CoSi)
120
122
136 (poly-Si)
118
poly-Si
116
SOI layer
114
BOX layer
Si-substrate
112
124
130 (CoSi)
2nd RTA

FIG. 2E

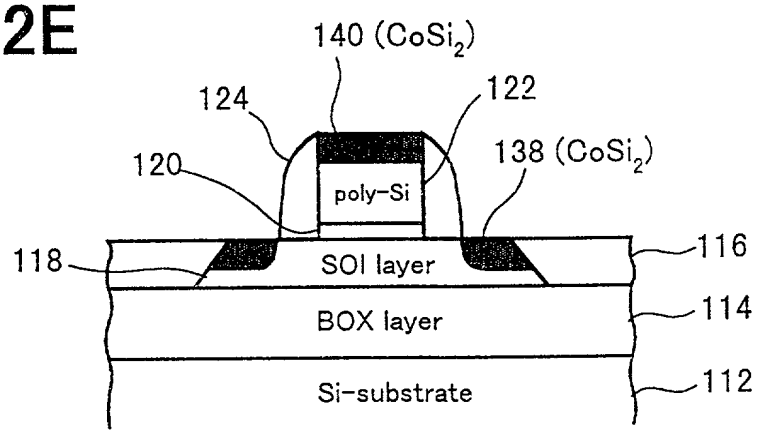

140 ($CoSi_2$)
124
122
120
138 ($CoSi_2$)
poly-Si
118
116
SOI layer
114
BOX layer
Si-substrate
112

FIG. 3A

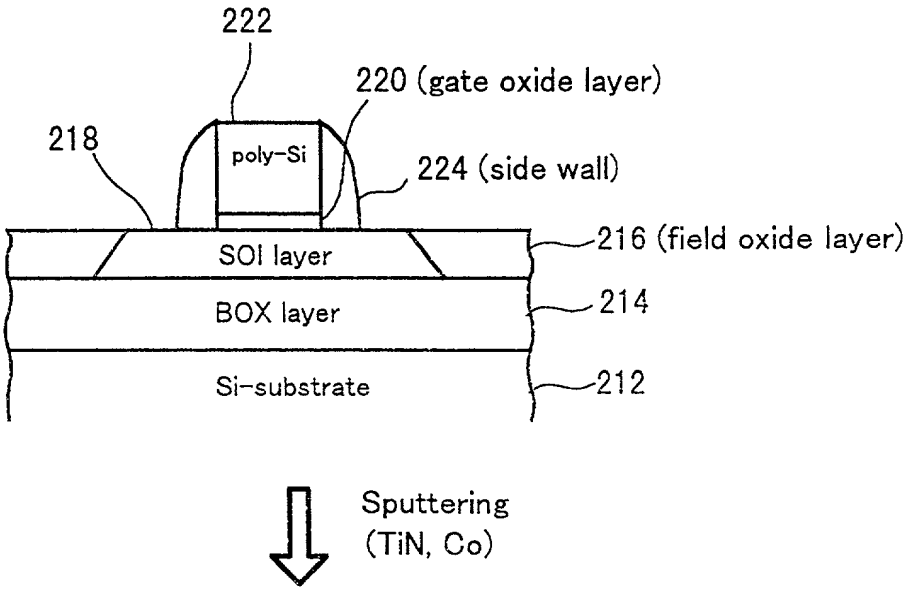


FIG. 3B

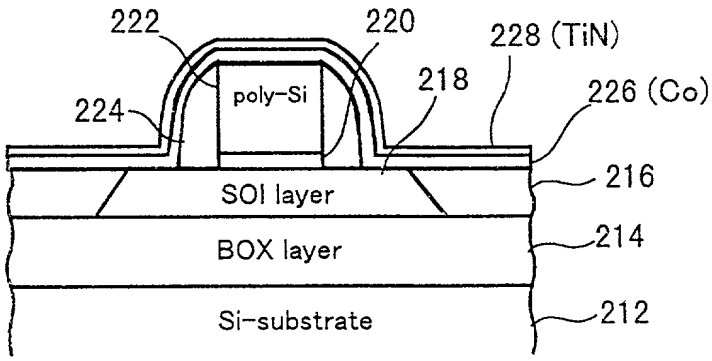


FIG. 3C

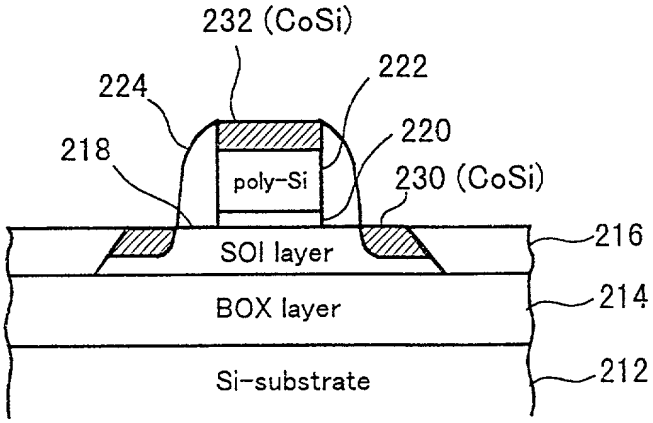
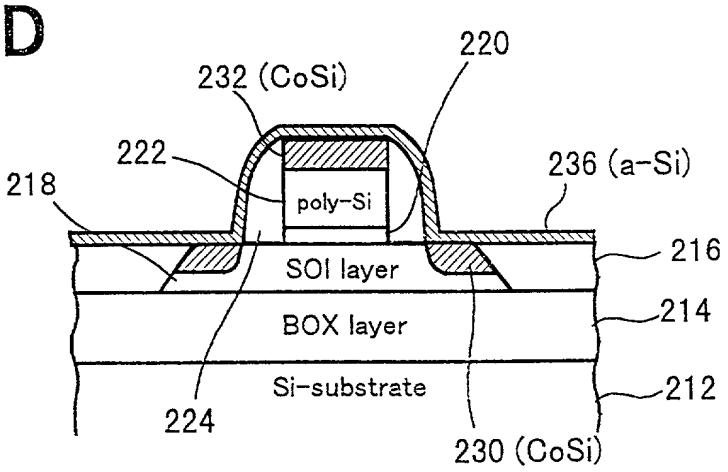


FIG. 3D



2nd RTA

FIG. 3E

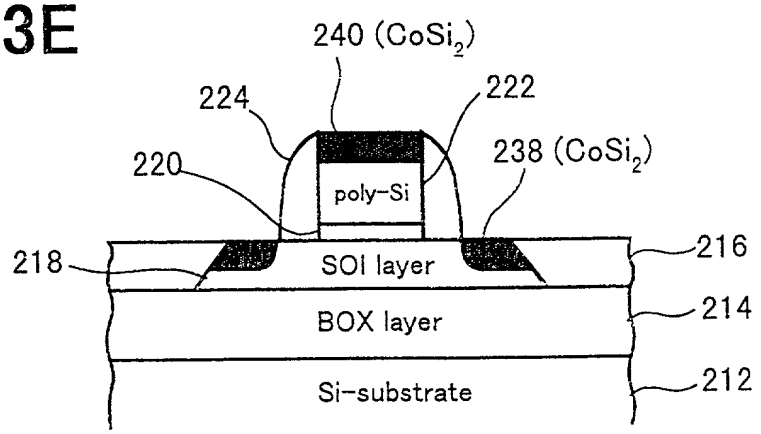


FIG. 4A

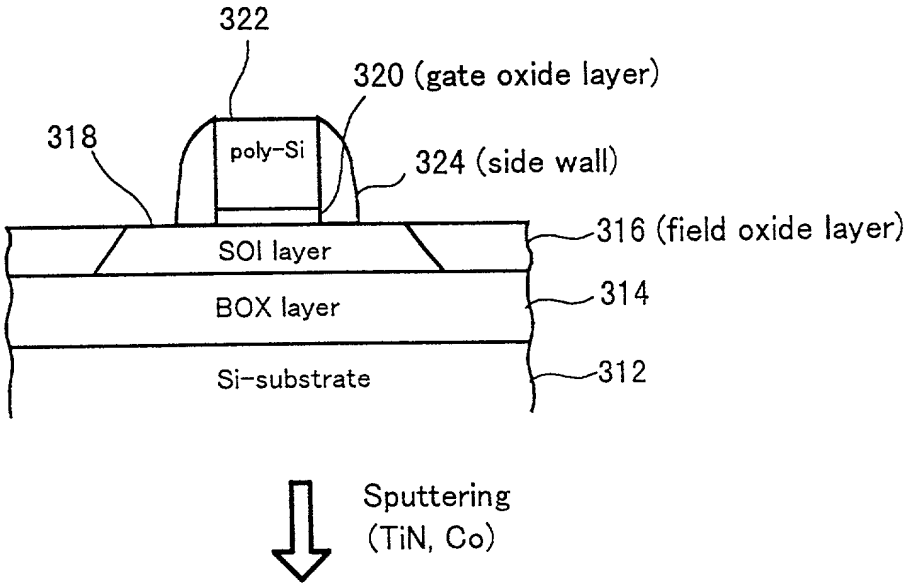


FIG. 4B

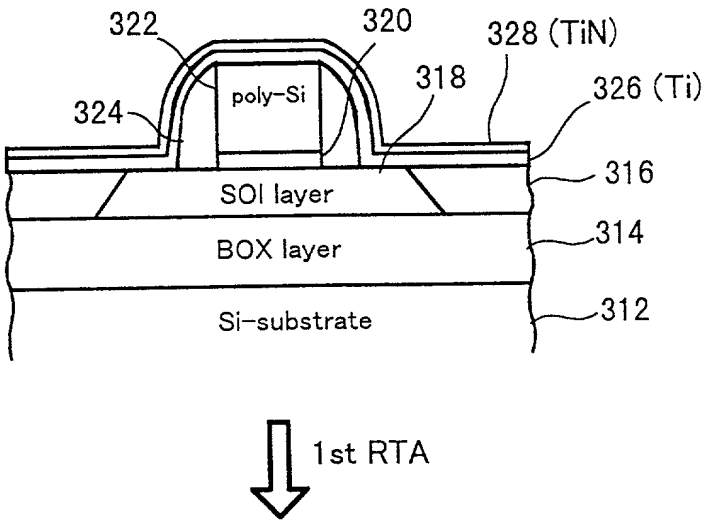


FIG. 4C

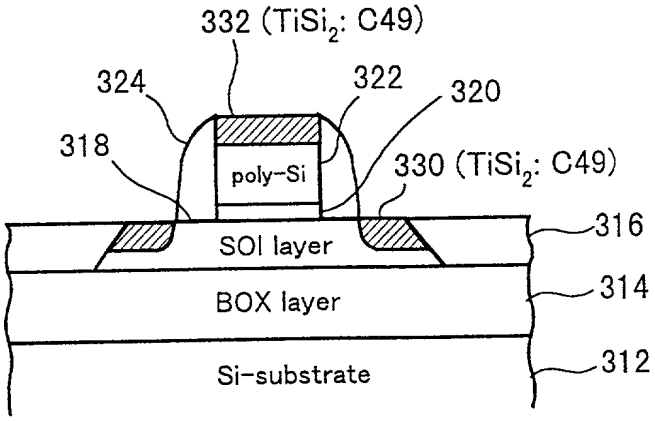


FIG. 4D

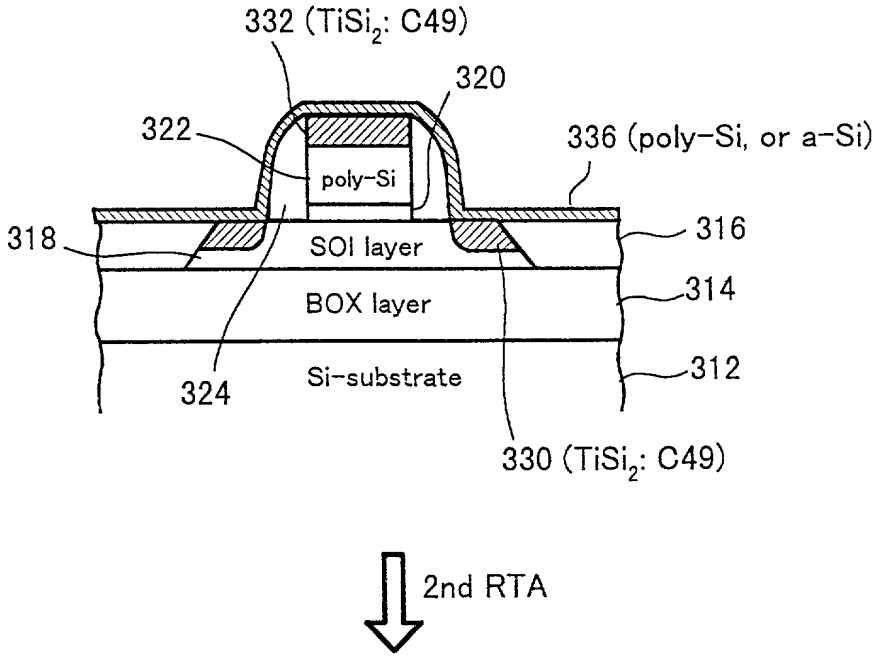

332 (TiSi2: C49)
320
322
336 (poly-Si, or a-Si)
poly-Si
318
SOI layer
316
BOX layer
314
Si-substrate
312
324
330 (TiSi2: C49)
2nd RTA

FIG. 4E

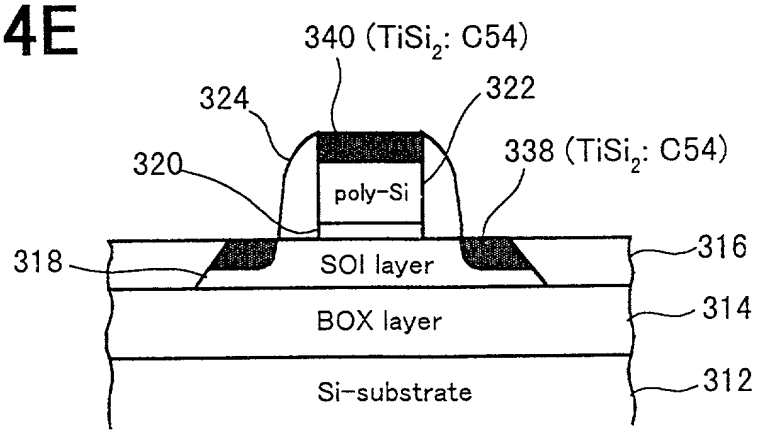

340 (TiSi2: C54)
324
322
320
338 (TiSi2: C54)
poly-Si
318
SOI layer
316
BOX layer
314
Si-substrate
312

FIG. 5A

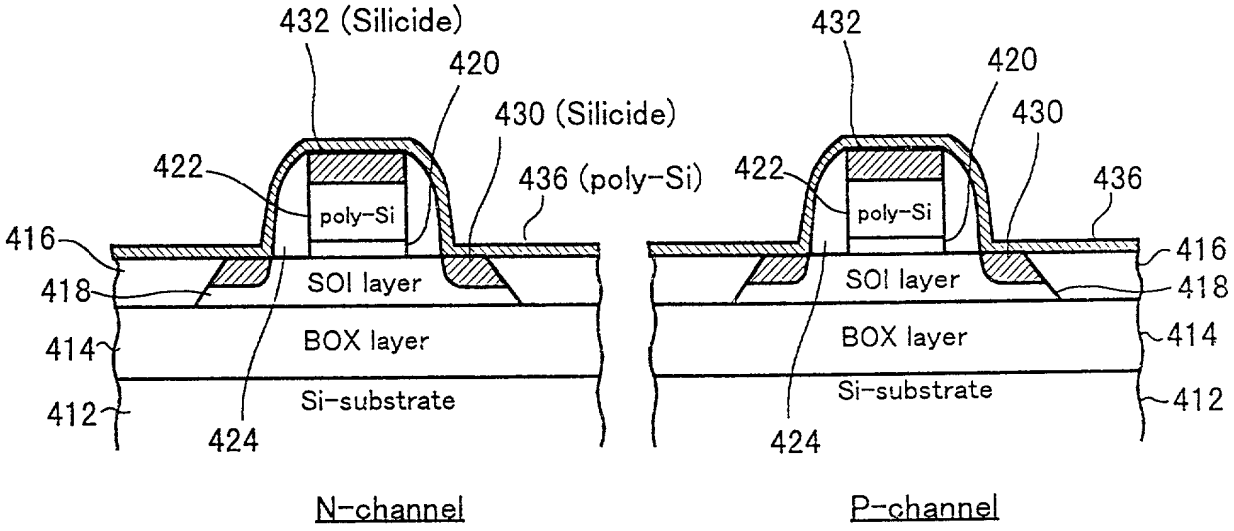

432 (Silicide)
420
430 (Silicide)
422
poly-Si
436 (poly-Si)
416
418
SOI layer
414
BOX layer
412
Si-substrate
424
N-channel
432
420
430
422
poly-Si
436
416
418
SOI layer
414
BOX layer
412
Si-substrate
424
P-channel

FIG. 5B

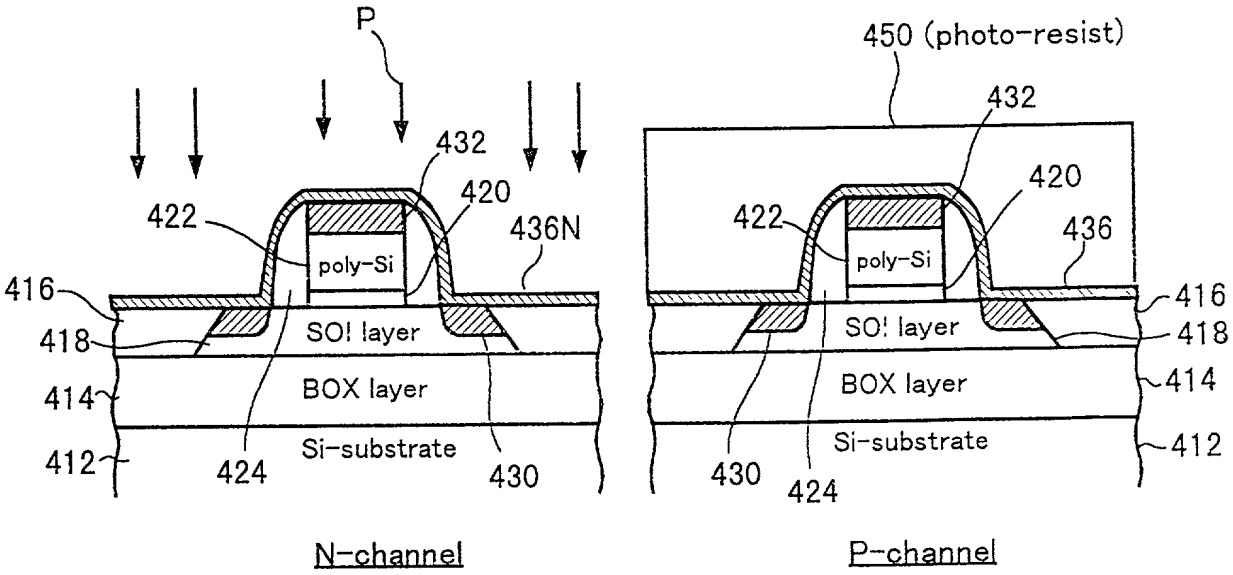
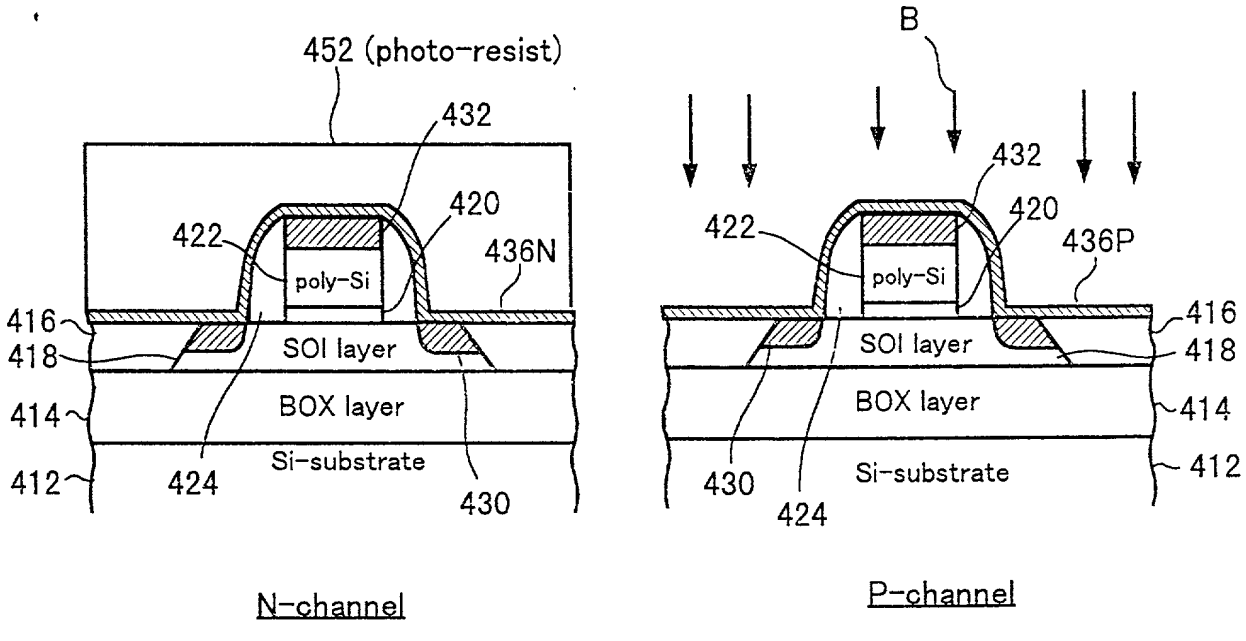

P
450 (photo-resist)
432
420
422
poly-Si
436N
436
416
418
SOI layer
414
BOX layer
412
Si-substrate
424
430
N-channel
P-channel

FIG. 5C



2nd RTA

FIG. 5D

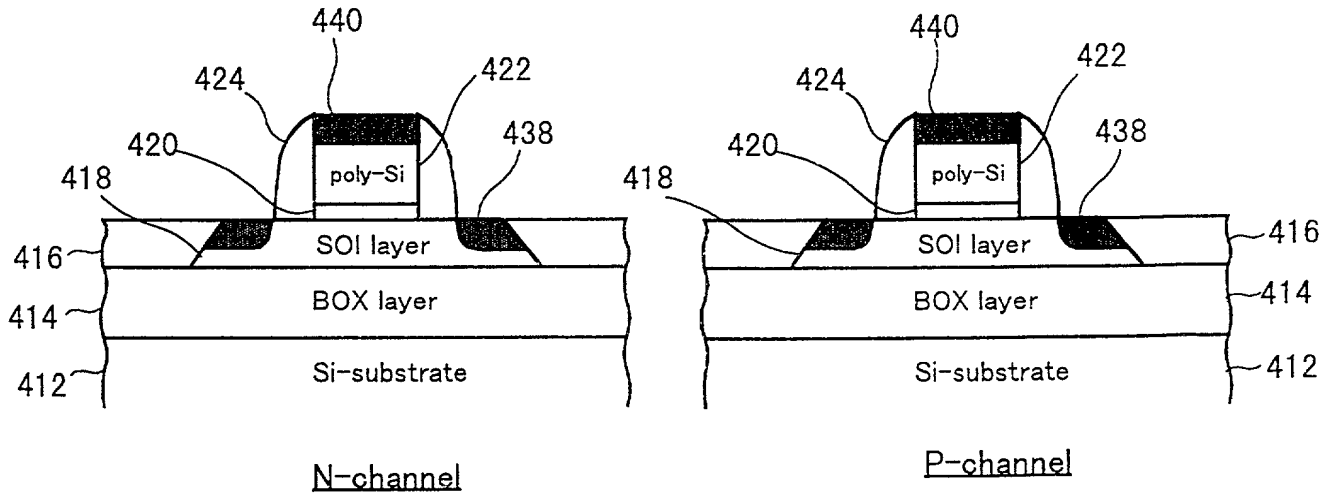


FIG. 6A

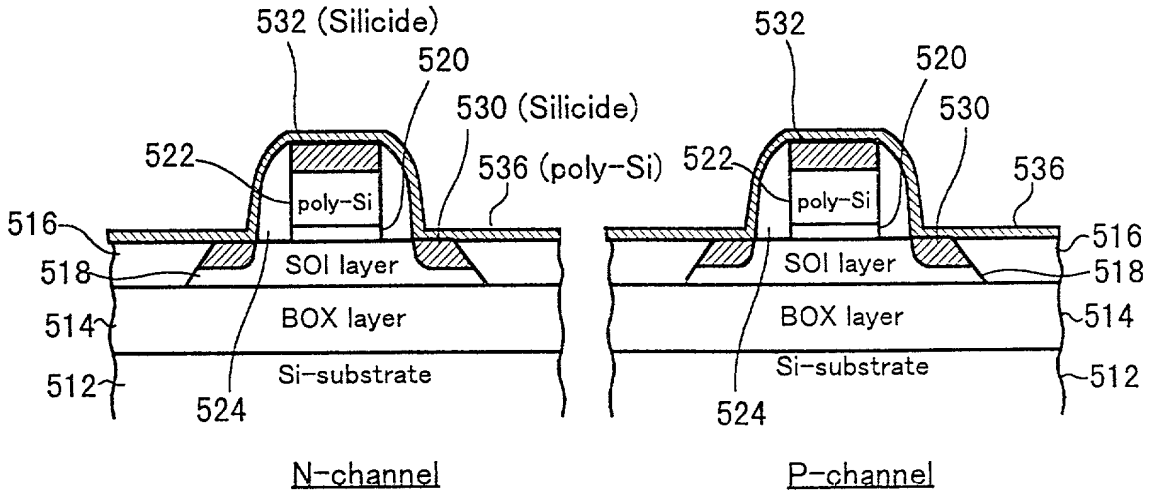


FIG. 6B

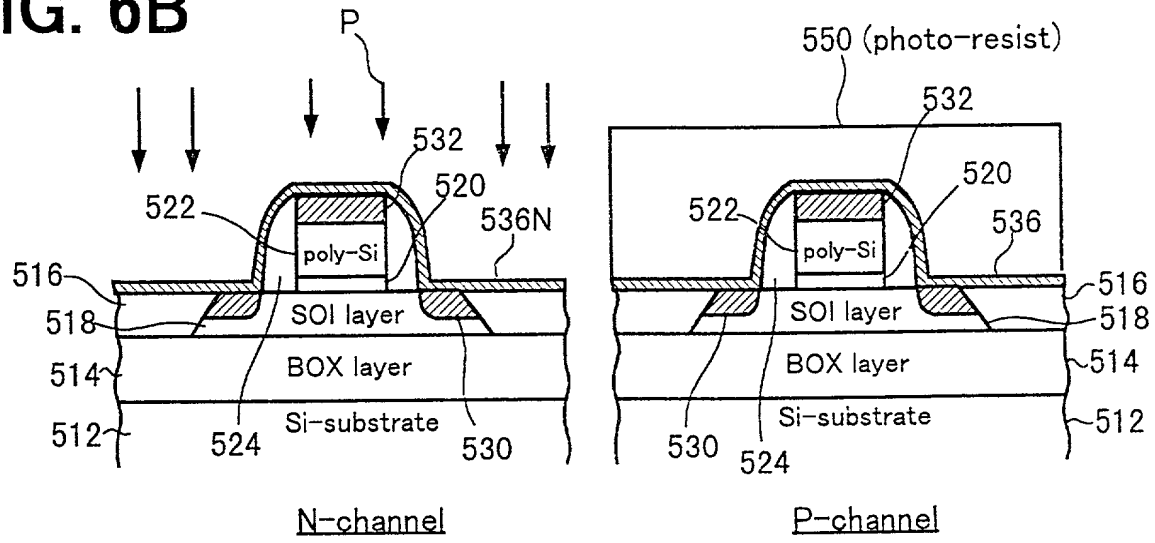
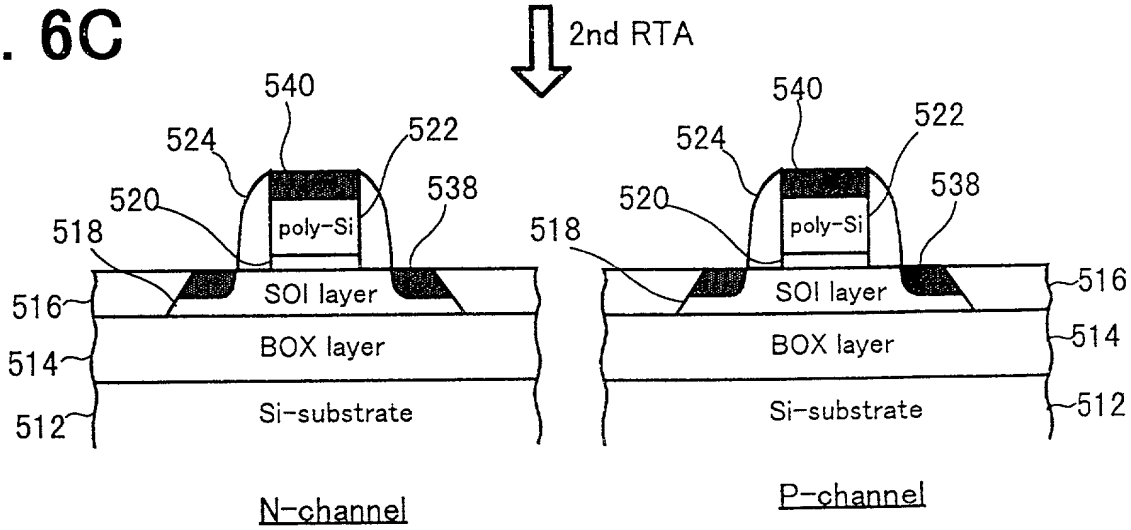


FIG. 6C



JONES & VOLENTINE, L.L.P. (8/97)

DECLARATION AND POWER OF ATTORNEY FOR U.S. PATENT APPLICATION

(x) Original ( ) Supplemental ( ) Substitute ( ) PCT ( ) Design

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that I verily believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

TITLE: Semiconductor Device and Method for Fabricating the Same

of which is described and claimed in:

(x) the attached specification, *or*

( ) the specification in the application Serial No._____ filed_____,

and with amendments through_____ (if applicable), *or*

( ) the specification in International Application No. PCT/_____, filed _____,

and as amended on _____ (if applicable).

I hereby state that I have reviewed and understand the content of the above-identified specification, including the claims, as amended by any amendment(s) referred to above.

I acknowledge my duty to disclose information of which I am aware which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, §119 (and §172 if this application is for a Design) of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

COUNTRY	APPLICATION NO.	DATE OF FILING	PRIORITY CLAIMED

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

APPLICATION SERIAL NO.	U.S. FILING DATE	STATUS: PATENTED, PENDING, ABANDONED

And I hereby appoint Raymond C. Jones, Reg. No. 34,631 and Adam C. Volentine, Reg. No. 33,289, members of the firm of JONES & VOLENTINE, L.L.P., jointly and severally, attorneys to prosecute this application and to transact all business in the U.S. Patent and Trademark Office connected therewith.

I hereby authorize the U.S. attorneys named herein to accept and follow instructions from IIZUKA & Co. as to any action to be taken in the U.S. Patent and Trademark Office regarding this application without direct communication between the U.S. attorneys and myself. In the event of a change in the persons from whom instructions may be taken, the U.S. attorneys named herein will be so notified by me.

Kindly direct all correspondence to: JONES & VOLENTINE, L.L.P.
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Reston, Virginia 20191

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Full Name of 2nd Inventor	FAMILY NAME	FIRST GIVEN NAME	SECOND GIVEN NAME
Residence & Citizenship	CITY	STATE OR COUNTRY	COUNTRY OF CITIZENSHIP
Post Office Address	ADDRESS	CITY	STATE OR COUNTRY ZIP CODE

Full Name of 3rd Inventor	FAMILY NAME	FIRST GIVEN NAME	SECOND GIVEN NAME
Residence & Citizenship	CITY	STATE OR COUNTRY	COUNTRY OF CITIZENSHIP
Post Office Address	ADDRESS	CITY	STATE OR COUNTRY ZIP CODE

Full Name of 4th Inventor	FAMILY NAME	FIRST GIVEN NAME	SECOND GIVEN NAME
Residence & Citizenship	CITY	STATE OR COUNTRY	COUNTRY OF CITIZENSHIP
Post Office Address	ADDRESS	CITY	STATE OR COUNTRY ZIP CODE

Full Name of 5th Inventor	FAMILY NAME	FIRST GIVEN NAME	SECOND GIVEN NAME
Residence & Citizenship	CITY	STATE OR COUNTRY	COUNTRY OF CITIZENSHIP
Post Office Address	ADDRESS	CITY	STATE OR COUNTRY ZIP CODE

I further declare that all statements made herein of my own knowledge are true, and that all statements on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

1st Inventor Jun Kanamori Jun KANAMORI Date June 9, 1999

2nd Inventor _____ Date _____

3rd Inventor _____ Date _____

4th Inventor _____ Date _____

5th Inventor _____ Date _____

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Applicant Reference No.:_____

Atty Docket No.:_____